Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Presently Amended) The memory error management method of Claim ~~1~~ 27 wherein said information is a plurality of bits in a memory controller buffer cell.

3. (Presently Amended) The memory error management method of Claim ~~1~~ 27 wherein said error checking and correction memory is a memory controller buffer of a disk array memory system.

4. (Presently Amended) The memory error management method of Claim ~~1~~ 27 wherein ~~said error correction process is~~ correcting the error in the information comprises using a single bit error correction code process that corrects a single bit error inline.

5. (Presently Amended) The memory error management method of Claim ~~1~~ 4 wherein the single bit error correction code process uses a hamming code and error syndrome ~~is utilized~~ to correct a bit in error.

6-7. (Canceled)

8. (Presently Amended) The memory error management method of Claim ~~1~~ 27 ~~wherein said memory cell error resolution process includes~~ further comprising a memory controller fail over process operable when, after rereading information from the error checking and correction memory at the location, it is determined that the correctable error has not been corrected and in which an alternate

memory controller buffer takes over master responsibilities associated with an overall memory input/output operation.

9-10. (Canceled).

11. (Presently Amended) A memory controller of Claim ~~10~~ 29 ~~wherein said~~ further comprising a controller processing core that directs the reader to ~~a~~ reread ~~of~~ the information from a physical memory medium when the error detector determines a non-correctable error exists and directs the writer to write the reread information ~~is utilized in said rewrite~~ to another location different from said location.

12. (Presently Amended) A memory controller of Claim ~~10~~ 29 ~~wherein said~~ further comprising a controller processing core that fences off said location and rewrites said information to a different location within said memory controller buffer when the error detector determines a non-correctable error exists.

13. (Presently Amended) A memory controller of Claim ~~9~~ 29 ~~wherein an error is detected and said~~ further comprising a controller processing core that relinquishes responsibility for master control operations to an alternate memory controller when the error detector determines a non-correctable error exists.

14. (Original) A memory controller of Claim 13 wherein an overall memory input/output operation that resulted in said error is treated as not complete and said processing core relinquishes responsibility for master control operations to an alternate memory controller that completes said overall memory input/output operation.

15. (Presently Amended) A memory controller of Claim ~~9~~ 13 wherein said

controller processing core receives responsibility for master control operations from another memory controller and processes a memory input/output operation request that produced an unrecoverable error.

16. (Presently Amended) A memory controller of Claim ~~9~~ 29 ~~further comprising~~ wherein the soft error corrector comprises and XOR array and an accumulator for storing information associated with the logic and arithmetic operations of said XOR array, said accumulator coupled to said XOR array.

17. (Presently Amended) The memory controller of Claim ~~7~~ 13 wherein said controller processing core directs tracking of error information including counts of soft correctable errors, hard correctable errors and non-correctable errors.

18-19. (Canceled)

20. (Presently Amended) A memory error resolution process of Claim ~~19~~ 30 wherein a soft correctable error handling process is engaged if ~~no errors exist after said re-checking information in said memory controller buffer~~ it is determined that the correctable error has been corrected.

21. (Original) A memory error resolution process of Claim 20 wherein a soft correctable error handling process comprises tracking soft correctable error information including incrementing a soft error correctable count.

22. (Presently Amended) A memory error resolution process of Claim ~~19~~ 30 wherein a hard correctable error handling process is implemented if ~~an errors exist after said re-checking information in said memory controller buffer~~ it is determined that the correctable error has not been corrected, said hard correctable error handling process includes an error fail-over process that utilizes resources of a different or alternate memory controller buffer.

~~22~~26. (Presently Amended) A memory error resolution process of Claim ~~19~~ 30 wherein said non correctable error handling process comprises:

fencing off ~~of a~~ the memory ~~controller buffer~~ location; and

~~forwarding the information to another location within a memory controller buffer~~ reading the information from another source and writing the information into the memory at another memory location different from the memory location.

23. (Presently Amended) A memory error resolution process of Claim ~~19~~ 30 wherein said non-correctable error handling process comprises an error fail-over process in which an initial memory controller that had control when a memory I/O operation resulted in a memory error relinquishes control to an alternate memory controller and said alternate memory controller attempts to complete said memory I/O operation.

24. (Presently Amended) A memory error resolution process of Claim ~~18~~ 30 further comprising performing a recursive error handling process.

25. (Presently Amended) A memory error resolution process of Claim ~~18~~ 30 further comprising performing a predictive failure analysis process.

27. (New) A memory error management method comprising:

reading information from an error checking and correction memory at a location;

if a correctable error exists in the information, correcting the error in the information;

rewriting the corrected information back into the memory at the location; and

rereading information from the error checking and correction memory at the location to determine whether the correctable error has been corrected.

28. (New) The memory error management method of claim 27 comprising reading the information from another source and writing the information into the memory at another location different from the location if a non-correctable error exists in the information.

29. (New) A memory controller comprising:

a memory controller buffer;

a reader that reads information from the memory controller buffer at a location;

an error detector that responds to the information by determining whether a correctable error exists;

a soft error corrector that cooperates with the error detector by correcting the correctable error in the information;

a memory refresher that writes the corrected information back into the memory at the location; and

a checker that cooperates with the memory refresher to cause the reader to read information from the memory controller buffer at the location to determine whether the correctable error has been corrected.

30. (New) A memory error resolution process operable in a memory in which an error has been discovered in information stored in a memory location, the process comprising:

if a correctable error exists in the information, correcting the error in the information, rewriting the corrected information back into the memory at the location and rereading information from the error checking and correction memory at the location to determine whether the correctable error has been corrected; and

if a non-correctable error exists in the information, performing a non-correctable error process.